REMARKS

Applicant requests the foregoing preliminary amendments be made to the application. In the event the Examiner believes a conference would serve to advance the prosecution of this application in any way, the undersigned attorney is available at the number noted below.

Respectfully submitted,

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I certify that the foregoing Amendment is being deposited with the United States Postal Service this 10th day of April 2002, in an envelope addressed to the U.S. Patent and Trademark Office, P.O. Box 2327, Arlington, Virginia 22202.

Joseph J. Zito 4/10/02
Date

Version With Markings To Show Changes Made To Claims 1-8

1. (amended) A system for allocating [millions of instructions per second (MIPS)] processing resources to functions in a queue waiting to be executed [in association with the information content of a number of communication channels], comprising:

a [digital signal processor (DSP)] processor having a queue for holding a plurality of executable functions including: [a number of communication ports each connected to a different one of said number of communication channels;]

a capacity determining means [within said DSP] for determining an amount of [MIPS] the processing resources that are available to be assigned;

a load determining means [within said DSP] for determining an estimate of [MIPS] the processing resources that are needed to execute each function waiting in the queue;

an allocating means [within said DSP] for allocating the [MIPS] processing resources to the functions based on a hierarchical priority scheme;

a measuring means connected to [said DSP] the processor for measuring an actual amount of the [MIPS] processing resources used;

a revising means [within said DSP] for revising the estimate of the amount of [MIPS] processing resources needed to execute each function waiting in the queue based on the measured amount of the [MIPS] processing resources used; and

a reallocating means [within said DSP] for reallocating the available amount of [MIPS] processing resources to the functions in accordance with the revised estimate and the hierarchical priority scheme.

2. (amended) The system of claim 1, further comprising:

a comparing means [within said DSP] for comparing the sum of the measured amount of [MIPS] processing resources used to a high and a low threshold value;

an alarming means interconnected with [said DSP] the processor for setting an alarm if the sum of the measured amount of [MIPS] processing resources used exceeds the high threshold value; and removing the alarm if the sum of the measured amount of [MIPS] processing resources used is less than the low threshold value.

3. (amended) The system of claim 2, further comprising:

a throttling means [within said DSP] for assigning a resource throttling value to each function waiting in the queue to be executed when the alarm is set, wherein the throttling value determines the reduction of the [MIPS] processing resources allocated to each of the functions.

4. (amended) The system of claim 2, further comprising:

a reducing means [within said DSP] for reducing a number of instances for which a particular function may execute concurrently when the alarm is set.

5. (amended) A system for allocating [memory] processing resources to functions in a queue waiting to be executed, comprising:

a [digital signal] processor [(DSP)] having [a number of] at least one communication port[s];

[a number of communication channels, each] at least one communication channel connected to [a different one of] each of said at least one communication port[s];

a capacity determining means [within said DSP] for determining an amount of [memory] processing resources available to be assigned;

a load determining means [within said DSP] for determining an estimate of [memory] processing resources needed to execute each function waiting in the queue;

an allocating means [within said DSP] for allocating the [memory] processing resources to the functions based on a hierarchical priority scheme;

a measuring means connected to [said DSP] the processor for measuring an actual amount of the [memory] processing resources used;

a revising means [within said DSP] for revising the estimate of the amount of [memory] processing resources needed to execute each function waiting in the queue based on the measured amount of the [memory] processing resources used; and

a reallocating means [within said DSP] for reallocating the available amount of [memory] processing resources to the functions in accordance with the revised estimate and the hierarchical priority scheme.

6. (amended) The system of claim 5, further comprising:

a comparing means [within said DSP] for comparing the sum of the measured amount of [memory] processing resources used to a high and a low threshold value;

an alarming means interconnected with [said DSP] the processor for setting an alarm if the sum of the measured amount of [memory] processing resources used exceeds the high threshold value and removing the alarm if the sum of the measured amount of [memory] processing resources used is less than the low threshold value.

7. (amended) The system of claim 6, further comprising:

a throttling means [within said DSP] for assigning a resource throttling value to each function waiting in the queue to be executed when the alarm is set, wherein the throttling value determines the reduction of the [memory] processing resources allocated to each of the functions.

8. (amended) The system of claim 6, further comprising:

a reducing means [within said DSP] for reducing a number of instances for which a particular function may execute concurrently when the alarm is set.